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TRANSMITTAL OF APPEAL BRIEF

Docket No. 594728821US

In re Application of: Lee et al.

Application No.	Filing Date	Examiner	Group Art Unit
10/045,601-Conf. #8571	November 7, 2001	P. M. Vital	2188

Invention: MULTISECTION MEMORY BANK SYSTEM

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: March 13, 2006 .

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Dated: October 2, 2006

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Express Mail No. EV 915639562 US

Docket No.: 594728821US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Lee *et al.*

Application No.: 10/045,601

Confirmation No.: 8571

Filed: November 7, 2001

Art Unit: 2188

For: MULTISECTION MEMORY BANK SYSTEM

Examiner: P.M. Vital

APPEAL BRIEF

Attention: Board of Patent Appeals
and Interferences
Assistant Commissioner for Patents
2011 Jefferson Davis Highway
Washington, D.C. 20231

Sir:

As required under 37 C.F.R. § 41.37(a), this brief is in furtherance of the Notice of Appeal in this application filed on March 13, 2006. The fees required under 37 C.F.R. § 41.20(b)(2), and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 (August 12, 2004). The complete Table of Contents follows.

CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Silicon Image, which is the assignee of record.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

Appellants, appellants' legal representative, and the real party in interest are unaware of any related appeals, interferences, or judicial proceedings that may be related to, directly affect, be directly affected by, or have a bearing on the Board's decision in the present appeal.

III. STATUS OF CLAIMS

Claims 1-22 are currently pending in this application. These claims stand rejected under 35 U.S.C. § 103(a).

Claims 7-22 are the subject of the present appeal.[1] The text of these claims is attached hereto as Appendix A.

IV. STATUS OF AMENDMENTS

Appellants have made no amendments subsequent to the final rejection of September 12, 2005 (hereinafter referred to as the "Final Office Action").

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Overview of the Invention[2]

Appellants' technology is directed to memory device technology that reduces the power consumption of a memory device and that facilitates the access of multiple hosts (e.g., any memory accessing device) to the memory device. *See, e.g.,* paragraphs 148, 159. Appellants' technology divides each section of data in a memory bank into multiple subsections, and allows each subsection to be selectively enabled or disabled. *See, e.g.,*

[1] Appellants are not appealing the rejection of claims 1-6 at this time to simplify the issues for this appeal. Appellants reserve the right to pursue these claims in a continuing application.

paragraph 159. For example, a memory bank section may have a word length of 64 bits. The section may be divided into two subsections of 32 bits each. *See, e.g.,* paragraph 159, Figure 36. Each of the subsections is enabled through a "section enable line" corresponding to that particular subsection. *See, e.g.,* paragraph 160. In some embodiments, the section enable line disables application of a row decoder signal to the memory section by logically "ANDing" the section enable signal and the output from the row decoder. *See, e.g.,* paragraph 160. When both 32-bit subsections are enabled, access to a memory location will access a 64-bit word. When only a single 32-bit subsection is enabled, access to the same memory location will only access a 32-bit word. Access is limited to the 32-bit word by disabling the subsection that isn't being accessed, and by latching the data from the subsection that has been enabled. *See, e.g.,* paragraph 160. As a result of this construction, power consumption is reduced since only certain subsections are enabled for access while the others may be disabled. Also as a result of this construction, multiple hosts may interact with the memory device in a manner that is optimized for the host, e.g., one host may require all subsections to be enabled while another host may only require certain subsections to be enabled.

B. Independent Claims on Appeal

The rejected independent claims are directed to memory device technology that allows memory subsections to be enabled or disabled. The independent claims are described as follows:

1. Claim 7

Claim 7 is directed to a memory bank having multiple sections, wherein each section represents a subdivision of a word of memory. *See, e.g.,* Figure 36 (3600, 3610), paragraph 159. A section and row enable lines to the section are only enabled when the subdivision of the word represented by the section is accessed. *See, e.g.,* Figure 36

[2] Copies of the application currently in appellants' possession have inconsistent line and page numbers. For the convenience of the Board, appellants have therefore cited to paragraph numbers from the corresponding Patent Application Publication US 2003/0208655 A1.

(3650, 3601, 3611), paragraph 160. Sections that are not enabled use less power than sections that are enabled. *See, e.g.,* paragraph 159.

2. Claim 15

Claim 15 is directed to a method of providing access to memory, wherein the memory includes multiple sections that each contain a subdivision of a word. *See, e.g.,* paragraph 159. An address to a word of memory to be accessed is received. *See, e.g.,* paragraph 160. A section of the memory, and row enable lines to the section, are disabled so that memory power is preserved when the subdivision of memory containing the addressed word is accessed. *See, e.g.,* Figure 36 (3601, 3611), paragraph 160.

3. Claim 20

Claim 20 is directed to a memory having a plurality of sections that each contain a subdivision of a word. *See, e.g.,* paragraph 159. Means for selectively disabling a section if the memory is provided when a word is accessed. *See, e.g.,* Figure 36 (3650, 3601, 3611), paragraph 160. When the word is accessed, a row enable line to the disabled section is not enabled. *See, e.g.,* Figure 36 (3601, 3611), paragraph 160. Moreover, when the word is accessed, power is saved because the section is disabled. *See, e.g.,* paragraph 159.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The Examiner's Rejections

The Examiner has rejected all of the pending claims pursuant to 35 U.S.C. § 103(a) on the following bases:

1. The Examiner has rejected claims 1-5, 7-13, 15 and 20 as being unpatentable over U.S. Patent No. 6,415,353 to Leung and U.S. Patent No. 4,797,850 to Amitai.

2. The Examiner has rejected claims 6, 14, 16-19 and 21-22 as being unpatentable over Leung, Amitai, and U.S. Patent No. 4,972,314 to Getzinger et al.

B. The Issues on Appeal

The issues on appeal, and the specific pending claims to which each relates, are:

1. Whether the combination of Leung and Amitai discloses or suggests a memory bank that enables access to a section of memory representing a subdivision of a word while not enabling access to another section of memory representing another subdivision of the word in order to use less power in the memory. The decision on this issue impacts all pending claims.

2. Whether the combination of Leung and Amitai discloses or suggests a memory bank wherein a row enable line to a section of memory is enabled when a subdivision of a word represented by the section is being accessed. The decision on this issue impacts all pending claims.

3. Whether the combination of Leung and Amitai discloses or suggests a memory bank wherein the memory bank supports a multiport mode of operation wherein sections of the memory bank representing a subdivision of a word of memory can be enabled on a port-by-port basis. The decision on this issue impacts claims 11, 13, 14, 16, 17 and 21.

VII. ARGUMENT

All of the pending claims have been rejected by the Examiner under 35 U.S.C. § 103(a) based on various combinations of U.S. Patent No. 6,415,353 to Leung (hereinafter "Leung"), U.S. Patent No. 4,797,850 to Amitai (hereinafter "Amitai"), and U.S. Patent No. 4,972,314 to Getzinger et al. (hereinafter "Getzinger"). Prior to distinguishing appellants' technology, a brief description of the Leung and the Amitai references will be provided.

A. The Leung Reference

Leung discloses a memory device containing memory cells that must be periodically refreshed in order to retain data values. Leung, 2:61-65. In one embodiment, the memory cells are DRAM (dynamic random access memory) cells. *Id.,* 2:65-66. The memory cells are arranged to form a plurality of independently controlled memory banks, each bank

associated with a corresponding access control circuit. *Id.,* 3:3-5, 7:5-10. It is advantageous to use DRAM cells because they are significantly smaller than SRAM (Static Random Access Memory). However, data stored on a DRAM cell must be periodically refreshed, which limits the external access time. *Id.,* 1:37-60. To overcome this limitation, Leung introduces an SRAM cache between the external data bus of the memory device and the DRAM memory banks. *Id.,* 3:21-23. The SRAM cache is sized to allow all write data to initially be written to the SRAM cache before being written to the memory banks, and all read data provided to the external data bus to be stored in the SRAM cache. *Id.,* 3:23-27. The use of the SRAM cache ensures that the DRAM memory banks are property refreshed within a predetermined refresh period in a manner that does not interfere with any read or write accesses to the memory cells. *Id., 3:28-35.*

In one embodiment of Leung, 64 memory banks are provided in the memory device. *Id.,* Figure 1, 7:4-7. Each of the memory banks are comprised of an array of 64 rows and 1024 columns of DRAM cells. *Id., 7:10-12.* Data may be read from one of the 64 DRAM banks at that same time as data is being written to another one of the DRAM banks. *Id.,* 7:16-60. Each memory bank is addressed first by bank (identifying one of the 64 memory banks), then by row (one of the 64 rows), then by section (the 1024 columns are divided into four 256-bit sections), then by word within each section (each 256-bit section is divided into eight 32-bit words). *Id.,* 7:48-57. Figure 3 of Leung is a schematic diagram of a single DRAM bank and associated access control circuit. *Id.,* Figure 3, 44-62. A row address decoder 205 is provided a 6-bit address (EA[10:5]) to select a memory row that is to be accessed within the DRAM memory bank. *Id.,*11:56-61, 13:31-32, 15:66-16:1, 16:21-23.

B. The Amitai Reference

Amitai discloses a DRAM (dynamic random access memory) controller that allows access to an individual byte of a multiple-byte data word. Amitai, 2:29-33. The DRAM controller provides a plurality of row address signals [RAS0-RAS3] to an array of memory banks 12A...12D. *Id.,* 3:12-14. Rather than applying a single column address strobe (CAS) to access an entire word in memory, the CAS is split to create separate CAS signals for the separate bytes of the data word. *Id.,* 2:32-49. For example, column address

signals [CAS0, CAS1] are applied to the memory bank to allow two different bytes of the memory to be accessed individually. *Id.*, 3:14-21.

C. Leung and Amitai Do Not Disclose Preserving Power by Not Enabling a Section of a Memory Bank Representing a Subdivision of a Word of Memory

All of the pending independent claims recite preserving power in a memory by only enabling access to a subdivision of a word of memory while disabling (or not enabling) access to other subdivisions of the word of memory. For example, claim 7 provides that the memory is comprised of a plurality of sections "each section represented a subdivision of a word of memory," wherein each section is "*selectively enabled*...when the subdivision of the word represented by the section is accessed...*so that sections that are not enabled* use less power than *sections that are enabled*" (emphasis added). Claims 15 and 20 contain similar limitations (and refer to "disabling" or "disabled" sections of memory). As is discussed above, one of the appellants' techniques for enabling or disabling a section of memory is to disable access to a subdivision of a word that would normally be retrieved from a particular address. For example, in the 64-bit embodiment discussed above, when both 32-bit subsections are enabled, access to a memory location will access a 64-bit word. When only a single 32-bit subsection is enabled, access to the same memory location will only access a 32-bit word.

None of the cited references discloses enabling and disabling access to a section of a memory bank representing a subdivision of a word of memory as disclosed by appellants. The Examiner primarily relies on Leung as disclosing the concept of selectively enabling or not enabling sections of memory in order to save power. *See, e.g.*, Final Office Action, page 5-6. The Examiner admits that Leung does not teach that each section of the memory represents a subdivision of a word of memory. *Id.*, page 6. The Examiner therefore relies on Amitai as disclosing that each section of a memory may represent a subdivision of a word in the memory. *Id.*, page 6.

Appellants respectfully submit that Leung and Amitai, either alone or in combination, do not disclose analogous structure or functionality to that claimed by appellants. In this regard, it is important to note that not enabling access to a section of memory is different

than not accessing a section of memory. In the former, access to the section of memory cannot be achieved even when that section of memory is being addressed. In the latter, access can be achieved, but is not done so because the memory location associated with a portion of the memory is not being addressed. Both Leung and Amitai operate in the latter fashion, that is, by limiting the access to memory locations within the device based on the utilized addresses. In Leung, data may be read from a memory address corresponding to one of the 64 DRAM banks. In Amitai, data may be read from an individual bit of a multiple-byte data word in memory based on a memory address. In contrast, appellants operate in the former fashion, not enabling access to selected memory locations. As will be discussed in further detail in Section D, one example of a structure provided by appellants for disabling access to a subsection of memory is a section enable line that can disable the row enable lines for that subsection. Appellants respectfully submit that there is no corresponding structure or functionality provided in Leung or Amitai that disables access to a portion of the memory. Leung and Amitai both fail to disclose disabling a section of the memory in a fashion that precludes data retrieval from the section and reduces power consumption.

Moreover, the technology disclosed in Leung or Amitai would not suggest appellants' solution. Leung's stated purpose is to enable a memory containing DRAM cells to operate like a SRAM device. Amitai's stated purpose is to enable addressing at the byte level. Neither suggest techniques for reducing power or allowing multiport operation as are claimed by appellants. Appellants therefore respectfully submit that one would not look to Leung or Amitai for possible solutions to the problem addressed by the appellants' technology. Since the Examiner has failed to present a *prima facie* case of obviousness, the pending claims should therefore be allowed.

D. Leung and Amitai Do Not to Disclose Disabling Row Enable Lines to a Section of a Memory Bank Representing a Subdivision of a Word of Memory

In addition to the broad concept of enabling and disabling access to a section of memory, appellants have also identified a novel technique to enable and disable such access. All of the pending independent claims recite selectively enabling one or more row

enable lines to a section representing a subdivision of a word of memory when the word is being accessed. For example, claim 7 states that "each section being selectively enabled so that row enable lines to a section are only enabled when the subdivision of the word represented by the section is accessed...." Claims 15 and 20 contain similar limitations. As is discussed above, in some embodiments a section enable signal is applied to an AND gate that is also coupled to the output from a row address decoder. When the section enable signal is low (or a logic "0"), the row decoder signal is not applied to the associated memory section and the section is therefore not accessible.

The Examiner relies on Leung as having disclosed a similar use of row enable signals and characterizes Leung as follows: "each section being selectively enabled so that row enable lines to a section are only enabled when the subdivision of the word represented by the section is accessed wherein only a portion of a word corresponding to enabled sections is accessible so that sections that are not enabled use less power than sections that are enabled." Final Office Action, page 5-6.

Appellants submit that the use of the row enable lines disclosed in Leung under normal memory accesses is not equivalent to "enabling" the row enable lines as claimed by appellants. As shown in Figure 3 of Leung, a row address decoder 205 is provided a 6-bit address (EA[10:5]) to select a memory row that is to be accessed within the DRAM memory bank. The row address decoder 205 selects the appropriate word line drivers 201 that allow read/write access to the DRAM cell array 200. Leung fails, however, to disclose or suggest a way to disable either the row address decoder 205 or the word line drivers 201 other than to not use the decoder or drivers to access a section of memory. In this regard, appellants submit that not using the row address decoder and word line drivers because the corresponding memory section is not being addressed is not the same as the method of enabling the word line drivers as is claimed by appellants. Since nothing in Leung discloses or suggests enabling or disabling the word line drivers in the manner claimed by appellants, nor can the normal of operation of the word line drivers as part of accessing the DRAM cell array be characterized as "not enabling" or "disabling" as

claimed by appellants, appellants submit that the Examiner has failed to present a *prima facie* case of obviousness. The pending claims should therefore be allowed.

E. Leung, Amitai, and Getzinger Do Not Disclose Allowing Subdivisions of a Word of Memory to be Enabled on a Port-by-Port Basis

Pending dependent claims 11, 14, 16, 17 and 21 each contain a limitation that the memory bank is part of a multiport memory device and the sections of the memory bank can be disabled on a port-by-port basis. For example, claim 11 states that "the memory bank is part of a multiport memory device and wherein the section enable lines are enabled based on the accessing port." Claims 14, 16, 17 and 21 contain similar limitations. As discussed above, one of the advantages of appellants' technology is that multiple hosts may interact with the memory device in a manner that is optimized for the host. For example, one host may require all subsections to be enabled while another host may require only certain subsections to be enabled.

The Examiner notes that Leung and Amitai do not teach disabling the sections of a memory bank on a port-by-port basis. Final Office Action, page 8. The Examiner therefore relies on Getzinger as disclosing memory storage divided into sections where "each section has a multiplexed input/output port that provides one of four data paths in order to provide a partitioned memory for the elimination of memory access contention." *Id.*, page 8.

Appellants respectfully submit that the rejection under the combination of Leung, Amitai, and Getzinger is improper for a number of reasons. First, the rejection is improper since the rejected claims 11, 14, 16, 17 and 21 depend from allowable independent claims 7, 15, and 20. As articulated above in sections C and D, Leung and Amitai do not disclose all of the limitations of appellants' independent claims. Second, the rejection is improper since Getzinger fails to disclose a structure analogous to that claimed by appellants. Getzinger discloses a technique to allow access to the same memory section by a number of attached arithmetic processors in order to eliminate memory access contention. Getzinger, 32:44-47. Allowing access to the same memory section is different than appellants claimed invention, which allows access to different sections of a memory

bank depending on the requirements of the attached host. For example, hosts that do not require access to a large amount of memory will have a portion of the memory disabled so that they cannot access that section. Finally, the rejection is improper because the Examiner has failed to identify a plausible suggestion or motivation in the prior art to combine Getzinger with Leung and Amitai. Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). In this regard, the Examiner contents that it would have been obvious to combine Getzinger with Leung and Amitai because "it was well know to provide a partitioned memory for elimination of memory access contention as taught by Getzinger." Final Office Action, p. 8. Appellants submit that even if the teachings of Getzinger were well known, it would not have been obvious to combine the reference with Leung and Amitai in order to arrive at appellants' solution because the problem of memory access contention being addressed by Getzinger is significantly different than the problem being addressed by appellants' claimed system (enabling flexibility by the accessing host). Because of the dissimilar nature of the problems addressed by each approach, it would not have been obvious to combine the references in the manner suggested by the Examiner. For all of the above reasons, the pending claims should therefore be allowed.

F. Obviousness Rejections over Leung and Amitai (Claims 7-13, 15 and 20)

Independent claims 7, 15, and 20, as well as claims 8-13 by virtue of their dependency, include the recitation of preserving power by not enabling a section of a memory bank representing a subdivision of a word of memory. The claims also recite not enabling row enable lines to the section of memory to disable the section. Specifically, claim 7 provides that each section of memory is "selectively enabled so that row enable lines to a section are only enabled when the subdivision of the word represented by the section is accessed wherein only a portion of a word corresponding to enabled sections is accessible so that sections that are not enabled use less power than sections that are enabled." Claim 15 provides for "disabling a section of memory...so that row enable lines

to the disabled section are not enabled when a word of memory is accessed" wherein an accessed section of memory does not include "the subdivision of the word in the disabled section of memory so that power is preserved by disabling the section of memory when access to the entire word is not needed." Claim 20 provides for "means for selectively disabling a section so that a row enable line to the disabled section is not enabled when a words is accessed...whereby power is saved because the section is disabled." As explained above in Sections C and D, these claims should be allowed because the combination of Leung and Amitai does not generally teach or suggest disabling a section of memory, nor specifically teach or suggest disabling the section of memory by disabling the row enable lines.

Dependent claim 11 contains the further limitation that "the memory bank is part of a multiport memory device and wherein the section enable lines are enabled based on the accessing port." As discussed above in Section E, this claim should also be allowed because Leung and Amitai do not disclose allowing subdivisions of a word of memory to be enabled on a port-by-port basis.

G. Obviousness Rejections Over Leung, Amitai and Getzinger (Claims 14, 16-19 and 21-22)

Claim 14 depends from independent claim 7, claims 16-19 from independent claim 15, and claims 21-22 from independent claim 20. These dependent claims should be allowed for the reasons set forth above with respect to the corresponding independent claims 7, 15, and 20.

In addition, claims 14, 16 and 21 contain the further limitation that the memory bank is part of a multiport memory device and the sections of the memory bank can be disabled on a port-by-port basis. As discussed above in Section E, these claims should also be allowed because Leung, Amitai, and Getzinger do not disclose allowing subdivisions of a word of memory to be enabled on a port-by-port basis and there is no suggestion to combine the references relied upon by the Examiner.

VIII. Summary

Appellants respectfully submit that the Examiner has failed to identify a combination of references that contains all of appellants' claim limitations. The Examiner has failed to show that Leung, Amitai, and Getzinger, either alone or in combination, discloses or suggests appellants' claimed system, or that there is a basis to combine Leung, Amitai, and Getzinger. Accordingly, appellants respectfully request reversal of the Examiner's rejections to claims 7-22.

Dated:

2 October 2006

Respectfully submitted,

By _____

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CLAIMS APPENDIX

Claims Involved in the Appeal of Application Serial No. 10/045,601

1 - 6. Not appealed.

7. (Previously presented) A memory bank having words that are addressable by addresses and having multiple sections, the memory bank comprising:

a plurality of sections, each section representing a subdivision of a word of memory, each word of memory being accessible via an address, each section being selectively enabled so that row enable lines to a section are only enabled when the subdivision of the word represented by the section is accessed wherein only a portion of a word corresponding to enabled sections is accessible so that sections that are not enabled use less power than sections that are enabled.

8. (Original) The memory bank of claim 7 wherein the address is divided into a row portion and a column portion and the memory bank includes a row decoder and a column decoder to selectively accesses a word of the memory bank.

9. (Original) The memory bank of claim 8 wherein output of the row decoder and output of the column decoder only drive sections that are enabled.

10. (Original) The memory bank of claim 9 wherein the outputs are buffered to accommodate row and column latencies.

11. (Original) The memory bank of claim 7 wherein the memory bank is part of a multiport memory device and wherein the section enable lines are enabled based on the accessing port.

12. (Original) The memory bank of claim 7 wherein different rows of different sections can be simultaneously accessed to satisfy different memory access requests.

13. (Original) The memory bank of claim 7 including configuration information storage for selectively enabling sections.

14. (Original) The memory bank of claim 13 wherein the memory bank is part of a multiport memory device and the selective enabling of sections is on a port-by-port basis.

15. (Previously presented) A method for providing access to memory, the method comprising:

disabling a section of the memory, the memory including multiple sections that each contain a subdivision of a word so that row enable lines to the disabled section are not enabled when a word of memory is accessed;

receiving an address for a word of memory that is to be accessed; and

accessing a subdivision of the addressed word of memory, the accessed subdivision not including the subdivision of the word in the disabled section of memory so that power is preserved by disabling the section of memory when access to the entire word is not needed.

16. (Previously presented) The method of claim 15 wherein the memory is a multiport memory and the sections can be disabled on a port-by-port basis.

17. (Previously presented) The method of claim 16 wherein different subdivisions of a word can be accessed through different ports.

18. (Previously presented) The method of claim 15 wherein the disabling of a section of the memory includes setting a configurable parameter of the memory.

19. (Previously presented) The method of claim 18 wherein the setting is stored in a latch that disables the section.

20. (Previously presented) A memory having words that are addressable by addresses, the memory comprising:

a plurality of sections that each contain a subdivision of each word; and

means for selectively disabling a section so that a row enable line to the disabled section is not enabled when a word is accessed and so that accesses to the memory access a subdivision of words that does not include the subdivision of the disabled section whereby power is saved because the section is disabled.

21. (Previously presented) The memory of claim 20 including a plurality of ports and wherein the means for selectively disabling does so on a port-by-port basis.

22. (Previously presented) The memory of claim 20 wherein the means for selectively disabling includes a latch for storing an indication of whether a section is disabled.

EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Examiner is being submitted.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.